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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,190	03/14/2001	Kazuyoshi Kawabe	501.39837X00	1717

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EXAMINER

LAO, LUN YI

ART UNIT PAPER NUMBER

2673

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/805,190

Applicant(s)

KAWABE ET AL.

Examiner

Lao Y Lun

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14, 16 and 20-24 is/are rejected.
- 7) ☒ Claim(s) 15 and 17-19 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Sakashita(6,501,451).

Sakashita teaches a display device comprising a display module(LCD display) and a correction circuit(see figures 1-5) for receiving a gradation signal (see figure 3 and column 7, lines 49), generating a correction signal for correcting luminance based on an (N-1th)(preceding frame) and an N-th frame(current frame) input gradation signal; correcting N-th frame input gradation signal using correctiong signal(6 or 207 or 407) and outputting the corrected N-th frame input gradation signal to an LCD display(see figures 2-5; column 5, lines 20-35 and column 8, lines 1-17).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1-14, 16 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Uehara et al(6,329,980) in view of Sakashita(6,501,451).

As to claim 1-14, 16 and 20-23, Uehara et al teach an display apparatus comprising a display module(e.g. LCD module); a correction circuit(10) for receiving a gradation signal(eg. Vd1-vd4)(see figures 3-4; column 3, lines 39-55 and column 11, lines 36-61); for increasing a gradation level of a current image signal if the current image signal is greater than the previous image signal(see figures 1, 4-6; column 1, lines 49-51 and column 9, lines 6-60); a data driver(36) applied the correct image signal to an image element and scan driver(35) selecting image element to which correcting signal is applied(see figure 4 and column 9, lines 6-19).

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Uehara et al fail to disclose a delay period is a frame period.

Sakashita teaches a delay period is an arbitrary constant time period(see figures 1-2; abstract; column 3, lines 27-40; column 5, lines 21-26 and column 7, lines 17-17-33). It would have been obvious to have modified with the teaching of Sakashita et al, since Uehara et al have been disclosed a delay period could be changed(see Uehara et al's column 7, lines 9-16); so as to increase the speed of displaying a high quality picture by extending the comparison period by one dot period to one frame period.

As to claims 3-5, Uehara et al teach a correction circuit(10) for decreasing a gradation level of a current image signal if the current image signal is less than the previous image signal(see figures 5-6).

As to claim 6, Sakashita teach an LCD display having a frame storage(203)(see figure 2).

As to claim 6, Uehara et al teach an adder/subtractor(4)(see figure 5).

As to claim 7, Uehara et al as modified by Sakashita teach the correction circuit(10) for generating a correction signal by linearizing the relationship between the correction signal and a gradation(see Uehara's figure 8(a)-8(g) and column 10, lines 9-49; and Sakashita's column 4, lines 937).

As to claims 7-8 and 22, it would have been obvious to have a compensation rate for luminance deficits in the correction signal is within 30%-10% for intermediate gradation in three-frame intervals since Sakashita teaches a display device for improve a display quality based on the difference of the

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luminance levels of present frame and the preceding frame(see figures 2-5; column 4, lines 9-37 and column 7, lines 17-33).

As to claims 9 and 23, Uehara et al teach the correction circuit comprising for edge enhancement(see figures 5-6 and column 9, lines 6-61).

As to claim 13, Uehara et al teach a timing control circuit(33)(see figure 4 and column 9, lines 6-13).

As to claims 14 and 16, Uehara et al teach a correction data table(132 or 325)(see figures 21, 25; column 17, lines 24-30 and column 20, lines 47-68).

As to claim 20-21, Uehara et al teach a correction circuit having a selection circuit(16)(see figure 10; column 11, lines 52-68 and column 12, lines 1-9).

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Uehara et al(6,329,980) in view of Sakashita(6,501,451) and Shimomura et al(5,406,305).

Uehara et al as modified fail to disclose a back-light.

Shimomura et al teach a display device comprising a back light(7)(see figure 1 and column 4, lines 4-26). It would have been obvious to have modified Uehara et al as modified with the teaching of Shimomura et al, so the display information could be viewed at night.

Allowable Subject Matter

6. Claims 15 and 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamazaki et al teach an LCD display having a subtraction circuit; a frame memory and an adder(403).

Shimada et al(6,219,017) teach an LCD display having a filed memory(8-1-8-3) and a correction circuit(7-1-7-3).

Furuhashi et al(6,556,180) teach an LCD display having a frame memory(104); comparator(106) and add/subtract circuit(108).

Okumura et al(JP 4-288589) teach an LCD display having a subtractor(2) and an adder(3)(see figure 1).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi, Lao whose telephone number is (703) 305-4873.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at (703) 305-4938.

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Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

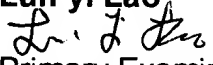
or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

August 16, 2004

Lun-yi Lao

Primary Examiner